Curriculum Vitae

I. Educations

University		Degree	Study Period	Major
KAIST (Former ICU)		B.S.	02/24/2003 – 06/15/2006	Electrical Communications Engineering
		M.S.	06/19/2006 – 02/14/2008	
University of Southern California (USC)		M.S.	08/27/2012 – 12/12/2018	Electrical Engineering
		Ph.D.	08/27/2012 – 08/06/2019	
Thesis Title	M.S.	Systematic power optimizing cyclic ADC design		
	Ph.D.	Energy-efficient design techniques and architectures for high-speed (GS/s) analog-to-digital converters		

II. Experience and Employment

Organization	Duration	Position	Activities and Responsibility	Location
ETRI	10/18/2006 – 10/17/2007	Part-time Researcher	CMOS low-power ADC design (ADC Architecture Development)	Daejeon, South Korea
	02/01/2008 – 06/18/2018 Leave of absence for Ph.D. degree (06/19/2012 – 06/18/2018)	Full-time Researcher	Sensor interface circuit design (Image/Audio/Display AFE)	Daejeon, South Korea
USC	08/25/2014 – 12/05/2014	Teaching Assistant (TA)	Mixed-Signal Integrated Circuit Design (EE536B)	Los Angeles, CA, US
	01/08/2017 – 04/27/2017			
Intel corporation	09/18/2017 – 12/29/2017	Intern	Next generation PCIe I/O PHY transceiver development	Santa Clara, CA, US
	09/23/2017 – 07/24/2020	Analog Engineer	Design wireline I/O circuits in Intel's leading-edge technology node	Hillsboro, OR, US
SeoulTech	**09/01/2020 – Present**	**Assistant Professor**	**Electronic & Information Engineering**	**Seoul, South Korea**

III. Honor and Award

Date	Type	Organization
04/17/2019	Outstanding student paper award (3rd place)	IEEE-CICC
08/24/2006	President award (Graduate with honor)	KAIST
04/03/2009	President award (Outstanding researcher)	ETRI
02/27/2012	Scholarship: Ph.D. Fellowship	USC Viterbi School of Engineering

IV. Academic Achievements

a) Journal and conference papers

	Authors, Title, journal, Vol., page and Year	Number of Authors	Role	Type	Note
1	S. Park, **J.-W. Nam**, and S. K. Gupta, "HW-BCP: A custom hardware accelerator for SAT suitable for single chip implementation for large benchmarks," the 26th Asia and South Pacific Design Automation Conf., Jan. 2021.	3	Co-Author	International Conference	Oral Presentation
2	H. W. Kwon, **J.-W. Nam**, and Y. K. Lee, "Generative adversarial attacks on fingerprint recognition systems," the 35th International Conf. on Information and networking (ICOIN), Jan. 2021.	3	Co-Author	International Conference	
3	**J.-W. Nam**, and Y. K. Lee, "Machine-learning based analog and mixed-signal circuit design and optimization," the 35th International Conf. on Information and networking (ICOIN), Jan. 2021.	2	Co-Author	International Conference	Poster Presentation
4	**J.-W. Nam**, and M.-W. Chen, "A 12.8-Gbaud ADC-based Wireline Receiver with Embedded IIR Equalizer," IEEE J. Solid-State Circuits, vol. 55, no. 3, pp. 557 – 567, Mar. 2020.	2	First Author	SCI Paper (IF=4.929)	
5	**J.-W. Nam**, and M.-W. Chen, "A 12.8-Gbaud ADC-based NRZ/PAM4 Receiver with Embedded Tunable IIR Equalization Filter Achieving 2.43-pJ/b in 65nm CMOS," IEEE Custom Integrated Circuits Conf., April. 2019.	2	First Author	International Conference	Outstanding Student paper Award

6	**J.-W. Nam**, M. Hassanpourghadi, A. Zhang, and S.-W. M. Chen, "A 12-bit 1.6, 3.2, and 6.4 GS/s 4-b/cycle Time-Interleaved SAR ADC with Dual Reference Shifting and Interpolation," IEEE J. Solid-State Circuits, vol. 53, no. 6, pp. 1765-1779, May 2018.	4	First Author	SCI Paper (IF=4.929)	
7	**J.-W. Nam**, and S.-W. M. Chen, "An embedded passive gain technique for asynchronous SAR ADC achieving 10.2 ENOB 1.36-mW at 95-MS/s in 65 nm CMOS," IEEE Trans. Circuits Syst. I, Reg. Papers, vol. 63, no. 10, pp. 1628 - 1638, Oct. 2016.	2	First Author	SCI Paper (IF=3.318)	
8	**J.-W. Nam**, M. Hassanpourghadi, A. Zhang, and S.-W. M. Chen, "A 12-bit 1.6 GS/s interleaved SAR ADC with dual reference shifting and Interpolation achieving 17.8 fJ/conv-step in 65nm CMOS," in Proc. IEEE Symp. VLSI Circuits, Jun. 2016, pp.154–156.	4	First Author	International Conference	Oral Presentation
9	**J.-W. Nam**, D. Chiong, and S.-W. M. Chen, "A 95-MS/s 11-bit 1.36-mW asynchronous SAR ADC with embedded passive gain in 65 nm CMOS," IEEE Custom Integrated Circuits Conf., Sep. 2013, pp. 1–4.	3	First Author	International Conference	Oral Presentation
10	**J.-W. Nam**, M. Hassanpourghadi, A. Zhang, and S.-W. M. Chen, "Low-power High Dynamic-range ADC with over GHz Bandwidth using Cost-efficient Multi-bit/cycle SAR ADC," GOMATech 2018.	4	First Author	Government Conference	
11	M. Hassanpourghadi, Q. Zhang, P. Sharma, **J.-W. Nam**, S. Su, S. Chowdhury, M.S.W. Chen, Sandeep Gupta, A.F.J. Levi, W. Handford, and W. Taylor, "Automated analog mixed signal IP generator for CMOS technologies," GOMATech 2019.	11	Co-Author	Government Conference	
12	Y.-D. Jeon, **J.-W. Nam**, K.-D. Kim, T. M. Roh, and J.-K. Kwon, "A dual-channel pipelined ADC with sub-ADC based on flash–SAR architecture," IEEE Trans. Circuits Syst. II, Exp. Briefs, vol. 59, no. 11, pp. 741–745, Nov. 2012.	5	Co-Author	SCI Paper (IF=2.45)	
13	Y.-K. Cho, Y.-D. Jeon, **J.-W. Nam**, and J.-K. Kwon, "A 9-bit 80 MS/s successive approximation register analog-to-digital Converter with a capacitor reduction technique," IEEE Trans. Circuits Syst. II, Exp. Briefs, vol. 57, no. 7, pp. 502–506, Jul. 2012.	4	Co-Author	SCI Paper (IF=2.45)	
14	Y.-K. Cho, Y.-D. Jeon, **J.-W. Nam**, and J.-K. Kwon, "A 10-bit 30-MS/s successive approximation register analog-to-digital converter for low-power sub-sampling applications," Elsevier Microelectronics Journal, vol. 42, no. 12, pp. 1335–1342, Jul. 2011.	4	Co-Author	SCIE Paper	
15	**J.-W. Nam**, Y.-D. Jeon, S.-J. Yun, T. M. Roh, and J.-K. Kwon, "A 12-bit 100-MS/s pipelined ADC in 45-nm CMOS," in Proc. IEEE ISOCC, 2011, pp. 405–407.	5	First Author	International Conference	Poster Presentation
16	**J.-W. Nam**, Y.-D. Jeon, Y.-K. Cho, J.-K. Kwon, "A 12-Bit 200-MS/s pipelined A/D converter with sampling skew reduction technique," *Elsevier Microelectronics Journal*, no. 11, vol. 42, pp. 1225-1230, Nov. 2011.	4	First Author	SCIE Paper	
17	Y.-D. Jeon, Y.-K. Cho, **J.-W. Nam**, W.-Y. Lee, K.-T. Hong, and J.-K. Kwon, "A 9.15mW 0.22mm^2 10b 204MS/s pipelined SAR ADC in 65nm CMOS," IEEE Custom Integrated Circuits Conf., Sep. 2010, pp. 1–4.	6	Co-Author	International Conference	Oral Presentation
18	**J.-W. Nam**, Y.-D. Jeon, Y.-K. Cho, S.-G. Lee, and J.-K. Kwon, "A 2.85mW 0.12mm^2 1.0V 11-bit 20-MS/s algorithmic ADC in 65nm CMOS," in Proc. IEEE ESSCIRC, 2009, pp. 468–471.	5	First Author	International Conference	Oral Presentation
19	Y.-D. Jeon, Y.-K. Cho, **J.-W. Nam**, S. -C, Lee, and J.-K. Kwon, "A 1.2 V 12 b 60 MS/s CMOS analog front-end for image signal processing applications," Elsevier ETRI Journal, vol. 31, no. 6, Dec. 2009.	5	Co-Author	SCIE Paper	
20	H. B. Le, **J.-W. Nam**, S.-T. Ryu, and S.-G. Lee, "Single-chip A/D converter for digital microphones with on-chip preamplifier and time-domain noise isolation," Electronics Letter, vol. 45, no. 3, pp. 151-153, 2009.	4	Co-Author	SCI Paper (IF=1.232)	
21	H.-B. Le, **J.-W. Nam**, S.-T. Ryu, and S.-G. Lee, "A CMOS sigma-delta modulator for a digital electret microphone with a high input-impedance preamplifier," 15th Korean Conf. on Semiconductors, Phyeong-Chang, Feb. 2008.	4	Co-Author	Domestic Conference	Poster Presentation

b) Patents (ending Patents are excluded)

	Name of the Patent, Inventor, Registration No., Date of the Registration	# of Inventors	Participation Rate (%)	Country of Registration	
				South Korea	US
1	Apparatus and method for reducing a noise in an output waveform using a multi-bit sigma-delta modulator and a three phase inverter,	4	40	√	√

	Jaewon Nam, Minki Kim, Jimin Oh, Yil suk Yang, KR101854395B1, May 8, 2018, US9350226B2, May 24, 2016.				
2	Sensorless BLDC motor systems and driving methods of sensorless BLDC motor, Young Kyun Cho, Hui Dong Lee, **Jaewon Nam**, Jong-Kee Kwon, KR101803384B1, Nov. 30, 2017, US8836259B2, Sept. 16, 2014.	4	10	√	√
3	Triangular wave generator and method generating triangular wave thereof, Hui Dong Lee, **Jaewon Nam,** Young Kyun Cho, Jong-Kee Kwon, Yil suk Yang, Jongdae Kim, KR101801199B1, Nov. 24, 2017, US8604845B2, Dec. 10, 2013.	6	10	√	√
4	Motor control device and method of controlling the same, **Jaewon Nam**, Young Kyun Cho, Hui Dong Lee, Yil suk Yang, Jong-Kee Kwon, Jongdae Kim, KR101739911B1, May 26, 2017, US9490734B2, Nov. 8, 2016.	6	50	√	√
5	Pipelined analog digital convertor, **Jaewon Nam**, Young Deuk Jeon, Young Kyun Cho, Jong-Kee Kwon, US8564469B2, Oct 22, 2013.	4	40		√
6	Reference voltage supply circuit including a glitch remover, Young Deuk Jeon, Young Kyun Cho, **Jaewon Nam**, Jong-Kee Kwon, US8547081B2, Oct. 1, 2013.	4	10		√
7	Successive approximation register analog-digital converter and method for operating the same, Young Kyun Cho, Young Deuk Jeon, **Jaewon Nam**, Jong-Kee Kwon, KR101309837B1, Sept. 23, 2013, US8164504B2, Apr. 24, 2012.	4	10	√	√
8	Analog digital converter, Young Deuk Jeon, Young Kyun Cho, **Jaewon Nam**, Jong-Kee Kwon, US8531328B2, Sept 10, 2013.	4	10		√
9	Pipelined analog digital converter, **Jaewon Nam**, Young Deuk Jeon, Young Kyun Cho, Jong-Kee Kwon, US8508392B2, Aug 13, 2013.	4	70		√
10	Analog digital converting device, Young Kyun Cho, Young Deuk Jeon, **Jaewon Nam**, Jong-Kee Kwon, US8362938B2, Jan. 29, 2013.	4	10		√
11	Pipeline analog-to-digital converter, **Jaewon Nam**, Young Deuk Jeon, Young Kyun Cho, Jong-Kee Kwon, KR101224102B1, Jan. 21, 2013, US8164497B2, Apr 24, 2012.	4	70	√	√
12	Digital-to-analog converter, Young Kyun Cho, Young Deuk Jeon, **Jaewon Nam**, Jong-Kee Kwon, KR101201892B1, Nov. 16, 2012, US8059022B2, Nov. 15, 2011.	4	10	√	√
13	Read-out circuit with high input impedance, Minhung Cho, Yi Gyoung Kim, **Jaewon Nam,** Jong-Kee Kwon, KR101183986B1, Aug. 19, 2012, US8300850B2, Oct. 30, 2012.	4	5	√	√
14	Successive approximation register analog-digital converter and method of driving the same, Young Kyun Cho, Young Deuk Jeon, **Jaewon Nam**, Jong-Kee Kwon, KR101182402B1, Sept. 13, 2012.	4	10	√	
15	Band-gap reference voltage generator, Young Kyun Cho, Young Deuk Jeon, **Jaewon Nam**, Jong-Kee Kwon, US8058863B2, Nov. 15, 2011.	4	10		√
16	Multi-stage successive approximation register analog-to-digital converter and analog-to-digital converting method using the same, Young Deuk Jeon, Young Kyun Cho, **Jaewon Nam**, Jong-Kee Kwon, US7999719B2, Aug 16, 2011.	4	10		√
17	Multi-stage dual successive approximation register analog-to-digital convertor and method of performing analog-to-digital conversion using the same, Young Deuk Jeon, Young Kyun Cho, **Jaewon Nam**, Jong-Kee Kwon, US7978117B2, July 12, 2011.	4	10		√
18	Method of algorithmic analog-to-digital conversion and algorithmic analog-to-digital converter, Seung-Chul Lee, **Jaewon Nam**, Young Deuk Jeon, Jong-Kee Kwon, US7705764B2, Apr 27, 2010.	4	30		√

V. Research Experiences

	Project Title	Program/grantor	Period	Total Expenses	Form of Participation	Note
1	POSH (Posh Open Source Hardware) (FA8650-18-2-7853)	Defense Advanced Research Project Agency (DARPA), US	06/2018 – 08/2019	6	Participant	in millions of USD
2	Multi-Tier Reconfigurable Transceivers for Hand-Portable Radios and Micro Base Stations in Networked Warfare (N00014-11-1-0819)	Office of Naval Research (ONR), US	08/2012 – 08/2016	3.25		
3	High Voltage/Current Power Module and ESD for BLDC Motor (MKE-10035171)	Ministry of Knowledge Economy (MKE), South Korea	03/2010 – 02/2015	16,750	Researcher (Supervision Institution)	in millions of KRW
4	45nm Analog Circuit for Mixed-signal SoC (MKE-415106883)		03/2008 – 02/2010	13,650		
5	Electrical components/module for ubiquitous terminal (MKE-415100592)		03/2006 – 02/2010	49,200		

VI. Invited Talks

	Organization	Host	Date	Location
1	Qualcomm Atheros (Topic: Embedded Passive gain SAR ADC)	Dr. Su, David	08/2013	San Jose, CA, US
2	Dong-A University, ECE (Topic: Low-power ADC)	Dr. Kim, Chang-Wan	02/2015	Pusan, South Korea
3	Marvell Semiconductor Incorporation (Topic: ADC-based wireline receiver)	Dr. Gambhir, Manisha	10/2018	Santa Clara, CA, US
4	Georgia Tech, ECE (Faculty job interview) (Topic: Advanced High-speed ADC)	Dr. Wang, Hua	01/2019	Atlanta, GA, US
5	University of Washington Bothell, EE (Faculty job interview) (Topic: Advanced High-speed ADC)	Dr. Choi, Seungkeun	02/2019	Bothell, WA, US
6	Lawrence Berkeley National Laboratory (LBNL) (Job talk) (Topic: Low power ADC design technique)	Dr. Grace, Carl	05/2019	Berkeley, CA, US
7	Intel corporation (Job talk) (Topic: ADC-based wireline receiver)	Dr. O'mahony, Frank	06/2019	Hillsboro, OR, US
8	Dong-A University, ECE (Topic: GS/s ADC trends in high-speed transceiver)	Dr. Kim, Chang-Wan	10/2015	Pusan, South Korea
8	Electronics and Telecommunications Research Institute (Topic: 25Gbps High-speed PAM4 wireline transceiver)	Dr. Lee, Ja-Yol	10/2020	Daejeon, South Korea
9	The institute of Semiconductor Engineers (Topic: ADC-based wireline receiver)	ISE	12/2020	Seoul, South Korea

VII. Academic Mentoring Activities

	Topic	Student Name	Date	Current Affiliation (Title)
1	Analog-front-end circuits design (M.S. Direct Research at Dr. Chen's group)	Park, Jong	2014 Fall	LG Electronics, South Korea (Specialist at LG-CTO)
2	High resolution ADC Design in 14nm FinFET (M.S. Direct Research at Dr. Chen's group)	Ravindranath, Abhilash	2017 Spring	Ansys, Inc., US (Senior Application Engineer)
3	Mixed-signal integrated circuits for a testing (M.S. Direct Research at Dr. Chen's group)	Zhou, Ruohan	2017 Fall	Seeking Ph.D. Position
4	CMOS VLSI EDA tutoring	Park, Soowang	2018 Fall	University of Southern California (Ph.D. student)
5	CMOS circuit design and testing (USC-KAU Summer intern program)	Kwon, O-Sung	2019 Summer	Korea Aerospace University (Undergraduate student)